What is claimed is:

1. A method of diagnosing an error in combinational verification of a Boolean expression of a circuit and a specification of said circuit, comprising the steps of:

generating a first set of potential error sites causing a nonequivalence of said Boolean expression and said specification using a first technique that operates quickly;

generating a second set of potential error sites, smaller in number than said first set of potential error sites, using a second technique that operates on the first set of potential error sites, where said second technique is slower than said first technique but more accurate; and

proving that a specific potential error site, contained in said second set of potential error sites, is an actual error site.

2. The method of claim 1, wherein said first technique is a X-Based method.

3. The method of claim 1, wherein said first technique is a backtrace method.

4. The method of claim 1, wherein said first technique is a combination of a backtrace method and a X-based method.

5. The method of claim 1, wherein said second technique is a complementation method.

6. A method of proving that a potential error site is an actual error site causing a nonequivalence of an implementation circuit and a specification circuit, comprising the steps of:

inputting outputs of said specification circuit and said implementation circuit into a first miter circuit, that outputs a zero value if the outputs of the specification and implementation circuits are the same;

forming a modified implementation circuit used to test said potential error site by replacing said potential error site with a multiplexor with data inputs being an original input to the potential error site and its complement, where the control of said multiplexor is the output of said first miter circuit;

inputting outputs of said specification circuit and said modified implementation circuit into a second miter circuit, that outputs a zero value if the outputs of the specification and modified implementation circuits are the same;

checking if the output of the said second miter circuit is always zero;

determining that said potential error site is an actual error site when the output of the said second miter circuit is always zero.

7. An improved backtrace method of diagnosing an error in combinational verification of a circuit having sites containing logical gates, comprising the steps of:

generating and simulating a 32-bit vector;

reading the input and output of each gate of said logical gates and determining bits for which the input and the output of said particular gate are the same;

tagging said input by said bits of said vector;

performing a bit-wise OR of said tagged bits from each fanout at each gate to determine the contribution of each path connecting said logical gates.

8. An improved X-based analysis method of diagnosing an error in combinational verification of a circuit having sites containing logical gates, comprising the steps of:

dividing 32-bit words, serving as input vectors, into upper halves and lower halves;

storing a vector pair in identical bit positions within said upper and lower halves of a particular word, setting the upper and lower halves of said words as complements for a given input of said inputs, and setting the upper and lower halves of said words to be identical for other inputs of said inputs;

inputting said input vectors into said gate inputs and simulating all gates;

monitoring the gate outputs for each gate, going from the output of the circuit through to the inputs of the circuit, determining if the gate outputs are bit-wise the same as the gate inputs; and

incrementing a count value for each gate according to the number of said bits that are different.